ABSTRACT OF THE DISCLOSURE

A sense amplifier includes a feedback controlled bit line access scheme that feeds a sense amplifier output signal back to control operation of its associated bit line access transistor. This feedback may be implemented using a pair of inverter circuits each coupling a respective output signal to the control gate of the associated access transistor. Alternatively, the feedback may be implement using a logic gate which logically combines the sense amplifier output signals together to generate an output signal for controlling operation of both access transistors. The logic gate is preferably a NAND gate. The sense amplifier further includes a cross-connected feedback inversion circuit which inverts a sense amplifier output signal from a first latch inverter for application to a conducting line of a second latch inverter.